1. (Cancelled)

2. (Currently Amended) The integrated circuit ~~carrier device~~ of claim 16, wherein the raised pedestals have sidewalls with an angle (α) greater than 45 degrees with respect to a plane of the carrier device die paddle.

3. (Currently Amended) The integrated circuit ~~carrier device~~ of claim 16, wherein the raised pedestals each have a plane surface which is parallel to a plane of the chip connection area and each has an area for connection of a single bonding wire.

4. (Currently Amended) The integrated circuit ~~carrier device~~ of claim 16, wherein a height ~~(hp)~~ of each of the raised pedestals lies in the range between 1/10 and 1.5 times of a ~~chip~~ height of the semiconductor die.

5. (Currently Amended) The integrated circuit ~~carrier device~~ of claim 16, wherein a height ~~(hp)~~ of each of the raised pedestals lies in the range from 1/5 to twice a material thickness (h) of the carrier device.

6. (Currently Amended) The integrated circuit ~~carrier device~~ of claim 16, wherein the raised pedestals each represent a local deformation of the carrier device which is formed by a punch or a bending-off device.

7. (Currently Amended) The integrated circuit ~~carrier device~~ of claim 16, wherein the raised pedestals are formed by application of material to the carrier device.

8. (Currently Amended) The integrated circuit ~~carrier device~~ of claim 1, wherein a silver or gold finish is applied to the raised pedestals.

9. (Currently Amended) The integrated circuit carrier device of claim 16, wherein there is at least one unbonded raised pedestal on the carrier device.

10. (Cancelled)

11. (Cancelled)

12. (Cancelled)

13. (Currently Amended) The integrated circuit ~~carrier device~~ of claim 17~~1~~, where the raised pedestals make an angle (α) greater than 45 degrees with the plane of the carrier device at all sideswalls, with the sidewalls having rounded junctions parallel to the plane of the carrier device or being rounded as a whole.

14. (Currently Amended) The integrated circuit ~~carrier device~~ of claim 17~~1~~, where the height of the raised pedestals lies in the range between 1/10 of the die ~~chip~~ height and the die~~chip~~ height itself.

15. (Currently Amended) The integrated circuit ~~carrier device~~ of claim 11, where only in the areas of the raised pedestals, a finish, particularly silver or gold, is provided for bondability.

16.(New) An integrated circuit, comprising:

a semiconductor die;

a carrier device comprising a die paddle onto which the die is attached and a plurality of metallic leads each comprising an inner lead portion that extends to an outer lead portion, where a plurality of stamped pedestals are arranged on the carrier device exteriorly surrounding and adjacent to the die paddle;

a first bond wire extending from the die to a first of the plurality of stamped pedestals, and a second bond wire extending from the first of the plurality of stamped pedestals to an inner lead portion; and

a package that encapsulates the semiconductor die, the die paddle, the first and second bond wires and the inner lead portions.

17.(New) An integrated circuit, comprising:

a semiconductor die;

a metallic carrier device comprising a planar surface onto which the die is attached and a plurality of metallic leads each comprising an inner lead portion that extends to an outer lead portion, where a plurality of stamped pedestals are arranged on the carrier device exteriorly surrounding and adjacent to the planar surface; and

a first bond wire extending from the die to a first of the plurality of stamped pedestals, and a second bond wire extending from the first of the plurality of stamped pedestals to an inner lead portion.